

Design Content – the Key to the Next Generations of ASSPs and ASICs

By Jordan Selburn, Principal Analyst

Forecast

Frequency, Time Period

- Current year and 2-year forecast of design activity
- 5-year annual forecast of revenue and silicon production resulting from new designs

Measures

- Number of design win opportunities
- Associated product revenue

Regions, Markets

- Worldwide

Detail Level

- IP type (application standards, memory, interface)
- Top-level application

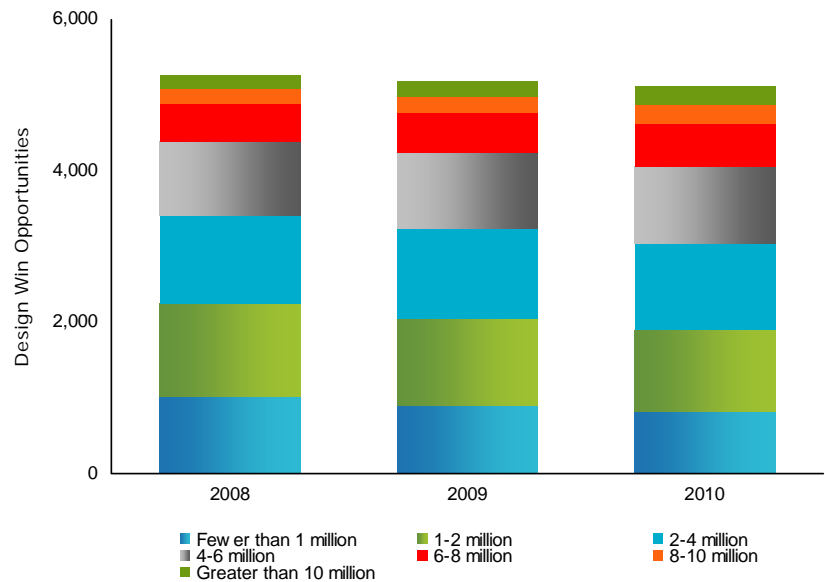
Technologies Covered

- ASSPs
- ASIC

Today's ASSP and ASIC designs can fit tens of millions of logic gates on a piece of silicon the size of a thumbnail. This incredible level of integration allows designers the ability to bring together the functions of an entire electronic system onto a single chip. To do so in a timely fashion – where “timely” is subject to ever shortening lifecycles – most designs are dependent upon the concept of design-reuse, in which some portions of the circuit design are pre-designed (often referred to as semiconductor Intellectual Property, or IP) and incorporated into the larger design as a functional block or interface. Much of this IP is acquired from third party providers, such as those identified in iSuppli's Design Infrastructure Report and Database.

As a key part of iSuppli's Semiconductor Design Service, the Design Content Database takes a detailed and comprehensive look into the heart of next generation ASSPs and ASICs. This research reveals the trends in application standards, memory and interface, providing developers, suppliers and users of semiconductor intellectual property critical market insights. The unique and flexible view into design requirements provided by the Design Content Database will enable a broad spectrum of participants in the semiconductor design chain to identify, target and capture the most attractive business opportunities.

New ASSP/ASIC Design Win Opportunities by Gate Count



Critical Questions Answered

- What IP will drive the next generation of semi-custom chip designs?
- How many designs will incorporate specific application standards, interfaces and memory types?
- What custom semiconductor revenue will be associated with various IP blocks and functions?

Who Should Use This Tool?

- ASSP Vendors, ASIC Vendors, PLD Vendors
 - Strategic Marketing
 - Product Marketing
- IP Providers, Design Service Companies
 - Product Marketing
 - Strategic Marketing
- Semiconductor Manufacturing Companies
 - Product Marketing
 - Partnership Managers

Lead Analyst

Jordan Selburn, Principal Analyst

Jordan Selburn is iSuppli's leading authority on semiconductor design including the trends and forecasts in the core silicon, System-on-a-Chip (SoC), Electronic Design Automation (EDA), and Intellectual Property (IP) space. Jordan is also iSuppli's expert in Set-Top Boxes (STBs) providing unique analysis and insight into all segments of the STB industry such as cable, satellite, Internet Protocol Television (IPTV) and terrestrial broadcast arenas.

Prior to joining iSuppli, Jordan served as the Director of Product Marketing for Amphion Semiconductor, where he was tasked with the management of the technical product market team. He launched products in all of Amphion's product families in addition to providing in-depth sales support for the products and the IP business model. Prior to his tenure with Amphion, Jordan was a Principal Analyst at Gartner Group/Dataquest.

Before his stint at Gartner Group/Dataquest, Jordan was the Marketing Manager and Product Line Manager at LSI Logic. Jordan has also had prior employment with Valid Logic Systems/Cadence Design Systems, Agilent/EEsof Inc. and Harris Corporation in various engineering capacities.

Jordan holds a Master of Science in Engineering Economic Systems from Stanford University in addition to a Master of Business Administration with distinction from Santa Clara University and a BSEE with honors from the University of Michigan.

Sample Database

Pivot Tables

ASSP/ASIC Design Win Opportunities
ASSP/ASIC Production Revenue (\$M)
ASSP/ASIC Unit Production (Units K)

Charts

Design-Chart
Revenue-Chart
Units-Chart