

New ASSP/ASIC Designs – The Roadmap to Opportunity

By Jordan Selburn, Principal Analyst

Forecast

Frequency, Time Period

- Current year and 2-year forecast of design activity
- 5-year annual forecast of revenue and silicon production resulting from new designs

Measures

- Number of design win opportunities
- Associated product revenue
- Associated silicon production
- Photomask requirements

Regions, Markets

- Worldwide

Detail Level

- Process node
- Top-level application

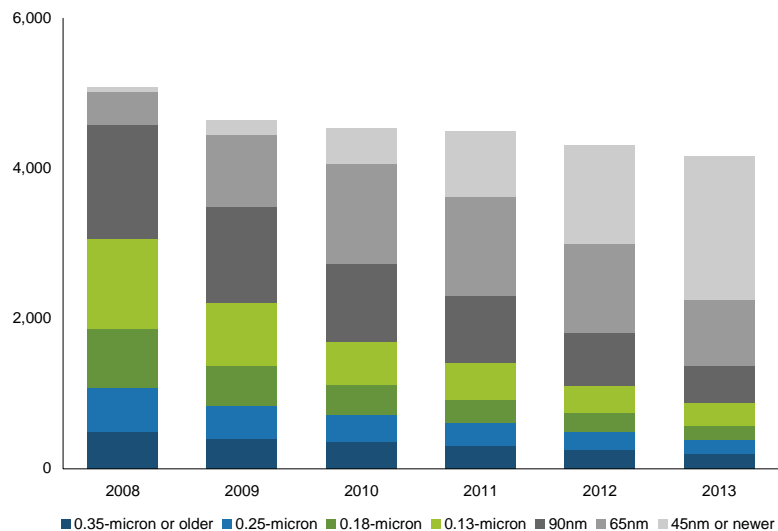
Technologies Covered

- ASSPs
- ASIC

The number of new ASSP and ASIC designs continues to decline each year. New process technologies such as 65 nanometer and 45 nanometer may bring greater integration, smaller size and lower power consumption than previous generations of silicon, but are burdened with higher design costs and greater levels of risk. At the same time, older process nodes such as 0.18-micron and 0.13-micron are still able to meet all the technical requirements for a majority of new chips, and as such are fully able to compete for the shrinking pool of new design opportunities alongside of the leading edge technologies. Unlike a decade ago, there are three, four or even more process nodes that are all experiencing significant design activity.

iSuppli's Design Win Opportunity Database takes a highly detailed look at current and expected ASSP and ASIC design activity. In addition to enumerating the current and forecast number of designs, this tool provides crucial data not before available, such as the revenue stream and silicon production associated with new designs. This information is critical for anyone associated or dependent upon new chip designs, allowing a wide range of professionals to identify real market opportunities and plan products to address those markets.

Number of New ASSP/ASIC Design Opportunities



Critical Questions Answered

- How many new ASSP and ASIC design win opportunities are there?
- What revenue will result from these new chip designs?
- What silicon production will result from these new chip designs?
- What application segments are driving the need for new chip design wins?
- How will design activity at new process nodes ramp, and how long will older nodes continue to show life?

Who Should Use This Tool?

- ASSP Vendor, ASIC Vendor, PLD Vendor
 - Strategic Marketing
 - Product Marketing
- IP Providers, Design Service Companies
 - Product Marketing
 - Strategic Marketing
- Semiconductor Manufacturing Companies
 - Product Marketing
- Manufacturing Infrastructure Companies
 - Product Marketing

Lead Analyst

Jordan Selburn, Principal Analyst

Jordan Selburn is iSuppli's leading authority on semiconductor design including the trends and forecasts in the core silicon, System-on-a-Chip (SoC), Electronic Design Automation (EDA), and Intellectual Property (IP) space. Jordan is also iSuppli's expert in Set-Top Boxes (STBs) providing unique analysis and insight into all segments of the STB industry such as cable, satellite, Internet Protocol Television (IPTV) and terrestrial broadcast arenas.

Prior to joining iSuppli, Jordan served as the Director of Product Marketing for Amphion Semiconductor, where he was tasked with the management of the technical product market team. He launched products in all of Amphion's product families in addition to providing in-depth sales support for the products and the IP business model. Prior to his tenure with Amphion, Jordan was a Principal Analyst at Gartner Group/Dataquest.

Before his stint at Gartner Group/Dataquest, Jordan was the Marketing Manager and Product Line Manager at LSI Logic. Jordan has also had prior employment with Valid Logic Systems/Cadence Design Systems, Agilent/EEsof Inc. and Harris Corporation in various engineering capacities.

Jordan holds a Master of Science in Engineering Economic Systems from Stanford University in addition to a Master of Business Administration with distinction from Santa Clara University and a BSEE with honors from the University of Michigan.

Sample Database

Pivot Tables

Design Win Opportunities
ASSP/ASIC Production
Photomasks

Charts

Design Win Opportunities Chart
ASSP_ASIC Production Chart
Photomasks Chart