

IC Price Evaluator

Unique View into Semiconductor Cost and Pricing

By Jordan Selburn, Principal Analyst

Critical Questions Answered

- What is today's street price for a custom chip, and how will that price change in the future?
- Approximately how much will it cost the manufacturer to build a particular chip, today and over the next several years?

Who Should Use This Tool?

- Purchasing
 - VPs, Directors, Managers
 - Commodity Managers
- Semiconductor IDM, Semiconductor Foundry
 - Marketing; Strategic Marketing or Business Development
 - Manufacturing, VPs/Directors

The IC Price Evaluator from iSuppli provides users with a detailed look into the economics of building and buying custom semiconductors. Through a simple, easy to understand user interface, purchasing specialists, commodity managers and other professionals involved in IC procurement can get valuable insight into their suppliers' cost base; the price that similar chips could be expected to sell for on the open market; as well as forecasts on how pricing will change in the future. This information can be of critical importance when negotiating the final sales contract, where a small reduction in chip price can result in the savings of millions of dollars.

iSuppli has crafted this tool to be usable by a wide range of people. While the modeling engine is very detailed, users only have to know a few basic parameters in order to use the model and get a unique view into semiconductor cost and pricing that can prove to be invaluable.

Annual 2007 to 2012 Pricing Analysis

Return to Pricing Selections
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Cost per Die, Yielded Wafer Cost, Gross Die and Die Yield						
	2007	2008	2009	2010	2011	2012
Open-Market Wafer Price:	\$620	\$639	\$633	\$655	\$658	\$674
Wafer Manufacturing Cost:	\$359	\$366	\$372	\$381	\$385	\$396
Gross Die:	213	213	213	213	213	213
Die Yield:	96%	96%	96%	96%	96%	96%
Net Die:	205	204	205	205	205	205
Mfg Price / Die:	\$3.02	\$3.14	\$3.09	\$3.20	\$3.21	\$3.29

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Modify Costs: 0.06 0.07 0.06 0.06 0.06 0.06

Royalties etc. / Die:	\$0.00	\$0.00	\$0.00	\$0.00	\$0.00	\$0.00
Wafer Sort / Die:	\$0.00	\$0.00	\$0.00	\$0.00	\$0.00	\$0.00
Packaging Price:						
Packaging Yield:						
Test Price:						
Test Yield:						
Finished Device Price:						

Pricing Mode Selections:

Year to model:	2007, 2008, 2009, 2010, 2011, 2012
Process to model:	0.7µm BCDMOS 3 150 nm Other French
Die Length:	8
Die Width:	8
Layer:	3
Yield model:	Exponential
Annual Production Volume:	500000
Type:	1
Volume:	High
Pins:	100

The tool supports a very wide range of process technologies, from 1.0-micron and older BiCMOS and BCD all the way through today's state-of-the-art 65-nanometer process. Packages include all industry standard choices, with options running the gamut from ceramic flip-chips to DIPs.

Lead Analyst

Jordan Selburn, Principal Analyst

Jordan Selburn is iSuppli's leading authority on semiconductor design including the trends and forecasts in the core silicon, System-on-a-Chip (SoC), Electronic Design Automation (EDA), and Intellectual Property (IP) space. Jordan is also iSuppli's expert in Set-Top Boxes (STBs) providing unique analysis and insight into all segments of the STB industry such as cable, satellite, Internet Protocol Television (IPTV) and terrestrial broadcast arenas.

Prior to joining iSuppli, Jordan served as the Director of Product Marketing for Amphion Semiconductor, where he was tasked with the management of the technical product market team. He launched products in all of Amphion's product families in addition to providing in-depth sales support for the products and the IP business model. Prior to his tenure with Amphion, Jordan was a Principal Analyst at Gartner Group/Dataquest.

Before his stint at Gartner Group/Dataquest, Jordan was the Marketing Manager and Product Line Manager at LSI Logic. Jordan has also had prior employment with Valid Logic Systems/Cadence Design Systems, Agilent/EEsof Inc. and Harris Corporation in various engineering capacities.

Jordan holds a Master of Science in Engineering Economic Systems from Stanford University in addition to a Master of Business Administration with distinction from Santa Clara University and a BSEE with honors from the University of Michigan.

Utilizes Two Costing Approaches

(1) Market-Based Price Engine

- Based on current and forecast wafer pricing, using iSuppli forecast of supply and demand at each process node
- Models the price that foundries are selling chips, and what fabless companies are paying
- Provides competitive benchmark for IDMs as well

(2) Market-Based Cost Engine

- Highly detailed calculation of manufacturing costs
- Behind the scenes factors include country-specific labor rates and depreciation schedules, raw materials costs, equipment costs
- Applicable for negotiations of very high-volume parts from suppliers with fabs

Model Inputs

- Process technology
- Wafer Fab
- Die size
- Annual production volume
- Package type and pin count
- Royalties and other per-chip payments

Model Outputs

- True wafer manufacturing cost for a given semiconductor fab
- Typical sales price of the wafer on the open market
- Gross die per wafer
- Chip yield
- Net good die per wafer
- True manufacturing cost of the die
- Typical sales price of similar chips on the open market
- Total device cost, including package, test and royalties

Deliverables

- Costing engines
 - Market-price
 - Silicon-price
- User's Guide
- Semi-annual updates
 - Reflects changes in the wafer market, device yield and fab utilization